# **EAST Search History**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1261	(375/341).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/03 12:57
<b>S2</b>	2	("6209209").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/03 12:59
S3	50	Hori and @pd="20010327"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/03 12:59
S4	2	S3 and viterbi	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/03 12:59
S5	2398	viterbi and (path near3 metric)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/04 13:03
S6	11	S5 and (adjustab\$5 near2 threshold)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/04 13:39
<b>S7</b>	2	("5341387").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/04 13:39
S8	1	(US-5341387-\$).did.	USPAT	OR	ON	2006/09/04 13:40
S9	0	S8 and S6	USPAT	OR	ON	2006/09/04 13:40
S10	1	S8 and "threshold"	USPAT	OR	ON	2006/09/04 14:55
S11	58	S5 and butterfly	USPAT	OR	ON	2006/09/04 14:55
S12	31	S11 and (number near4 metric)	USPAT	OR	ON	2006/09/04 18:42

# **EAST Search History**

S13	7	S12 and @pd<"20010123"	USPAT	OR	ON	2006/09/04 18:33
S14	565	S5 and (state adj2 transition)	USPAT	OR	ON	2006/09/04 15:21
S15	262	S14 and @pd<"20010123"	USPAT	OR	ON	2006/09/04 15:33
S16	15	S15 and (power near3 "2")	USPAT	OR	ON	2006/09/04 15:25
S17	7	S15 and (power adj3 "2")	USPAT	OR	ON	2006/09/04 15:29
S18	5	S5 and (threshold with power with "2")	USPAT	OR	ON	2006/09/04 15:32
S19	0	S5 and ("threshold is" with power with "2")	USPAT	OR	ON	2006/09/04 15:32
S20	0	viterbi and ("threshold is" with power with "2")	USPAT	OR	ON	2006/09/04 15:32
S21	0	viterbi and ("threshold is" same power same "2")	USPAT	OR	ON	2006/09/04 15:34
S22	154	viterbi and (threshold same power same "2")	USPAT	OR	ON	2006/09/04 15:33
S23	53	S22 and @pd<"20010123"	USPAT	OR	ON	2006/09/04 15:36
S24	2	("threshold is" same power same "2")	USPAT	OR	ON	2006/09/04 15:35
S25	0	("threshold is" with power with "2")	USPAT	OR	ON	2006/09/04 15:35
S26	3072	(threshold with power with "2")	USPAT	OR	ON	2006/09/04 15:35
S27	1785	S26 and @pd<"20010123"	USPAT	OR	ON	2006/09/04 15:40
S28	6	S27 and trellis	USPAT	OR	ON	2006/09/04 15:39
S29	17	S27 and viterbi	USPAT	OR	ON	2006/09/04 15:39
S30	0	S20 and "power of 2"	USPAT	OR	ON	2006/09/04 15:40
S31	0	"power of 2"	USPAT	OR	ON	2006/09/04 15:40
S32	0	"power of 2"	USPAT	OR	ON	2006/09/04 15:40
S33	56959	Power near2 "2"	USPAT	OR	ON	2006/09/04 15:40
S34	448	S33 and (viterbi or trellis)	USPAT	OR	ON .	2006/09/04 15:40
S35	185	S34 and @pd<"20010123"	USPAT	OR	ON	2006/09/04 16:51
S36	77	S35 and threshold	USPAT	OR	ON	2006/09/04 15:50
S37	1	(US-4879729-\$).did.	USPAT	OR	ON	2006/09/04 15:50
S38	41	S36 and (threshold same power)	USPAT	OR	ON	2006/09/04 15:51
S39	21	S36 and (threshold near7 power)	USPAT	OR	ON	2006/09/04 16:00
S40	370	(logic near3 value) near3 "OR"	USPAT	OR	ON	2006/09/04 16:01
S41	3	S40 and viterbi	USPAT	OR	ON	2006/09/04 16:01
S42	1	(US-5907586-\$).did.	USPAT	OR	ON	2006/09/04 16:48
S43	4	S5 and ((number near3 decision) SAME SNR)	USPAT	OR	ON	2006/09/04 16:51

# **EAST Search History**

S44	23	S5 and (decision adj2 depth) and SNR	USPAT	OR	ON	2006/09/04 16:51
S45	6	S44 and @pd<"20010123"	USPAT	OR	ON	2006/09/04 16:52
S46	21	S11 and @pd<"20010123"	USPAT	OR	ON	2006/09/04 18:33

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IEEE STD	IEEE Standard	Volume 36, Issue 6, 16 March 2000 Page(s):574 - 576 Digital Object Identifier 10.1049/el:20000444					
		AbstractPlus   Full Text: PDF(172 KB) IEE JNL					
		2. A VLSI implementation of an adaptive-effort low-power Viterbi decoder fo					

communications

Allan, G.; Simmons, S.;

Electrical and Computer Engineering, 2001. Canadian Conference on

Volume 2, 13-16 May 2001 Page(s):1183 - 1188 vol.2 Digital Object Identifier 10.1109/CCECE.2001.933609

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3. An efficient Viterbi decoder design for DMB receiver 

HyoWon Kim; BongSoo Lee; SuHyun Kim; SeongJun Shin; JoungChul Ahn; Intelligent Signal Processing and Communication Systems, 2005. ISPACS 200 2005 International Symposium on

13-16 Dec. 2005 Page(s):569 - 572

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IEEE CNF	IEEE Conference Proceeding	1. A low-power VLSI architecture for the Viterbi decoder					
IEE CNF	IEE Conference Proceeding	Wann-Shyang Ju; Ming-Der Shieh; Ming-Hwa Sheu; <u>Circuits and Systems, 1997. Proceedings of the 40th Midwest Symposiu</u> Volume 2, 3-6 Aug. 1997 Page(s):1201 - 1204 vol.2					
IEEE STD	IEEE Standard	Digital Object Identifier 10.1109/MWSCAS.1997.662295					
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		2. A low power survivor memory unit for sequential Viterbi-Decoder Traber, M.;  Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Volume 4, 6-9 May 2001 Page(s):214 - 217 vol. 4  Digital Object Identifier 10.1109/ISCAS.2001.922210  AbstractPlus   Full Text: PDF(356 KB) IEEE CNF  Rights and Permissions					
		3. VLSI implementation of a high-speed and low-power punctured Vi Li Qiao; You Yuxin; Wang Jinxiang; Ye Yizheng; TENCON '02. Proceedings. 2002 IEEE Region 10 Conference on Com Control and Power Engineering Volume 2, 28-31 Oct. 2002 Page(s):1205 - 1208 vol.2 AbstractPlus   Full Text: PDF(327 KB) IEEE CNF Rights and Permissions					
		4. VLSI design and implementation of high-speed Viterbi decoder Yu-xin You; Jin-xiang Wang; Feng-chang Lai; Yi-zheng Ye; Communications, Circuits and Systems and West Sino Expositions, IE Conference on Volume 1, 29 June-1 July 2002 Page(s):64 - 68 vol.1  AbstractPlus   Full Text: PDF(448 KB)   IEEE CNF Rights and Permissions	EE 2002				
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